28. The method of claim 26, wherein the substrate has an effective dielectric constant of no greater than about 5.

29. The method of claim 26, further comprising removing a contaminant on the substrate by:

a) introducing a reducing agent comprising nitrogen and hydrogen into a chamber;

b) initiating a reducing plasma in the chamber;

c) exposing an oxide on the substrate to the reducing agent.

30. The method of claim 24, further comprising filling the damascene structure with a liner layer and a conductive material to form a damascene feature.

31. The method of claim 30, further comprising depositing a silicon carbide barrier layer over the damascene feature.

REMARKS

This is intended as a full and complete response to the Office Action dated April 25, 2002, having a shortened statutory period for response set to expire on July 25, 2002. Claims 14-31 are pending in the application. Claims 14-31 were considered and are rejected by the Examiner. Applicants believe that no new matter has been introduced in this response.

Claims 14-28, 30, and 31 stand rejected under 35 U.S.C. § 103(a) as obvious over the combination of *Endo et al.* (US Patent No. 4,532,150), European Patent 0725440, *Wang et al.* (US Patent No. 4872947), *Somekh* (US Patent No. 6,291,334), and *Zhao* (US Patent No. 6,071,809). The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the silicon carbide deposition process of *Endo et al.* or European Patent 0725440 as the dielectric or barrier layers in the Applicants' prior art structure, form the silicon carbide layers *in situ* with other materials in view of the deposition processes in the disclosure of

Wang et al., and with the etch stops of *Somekh* and *Zhao* to enable the formation of the structure of Figure 1. Applicants respectfully traverse this rejection.

Endo et al. '150 discloses a process for depositing silicon carbide on a substrate. The substrate may be metallic, such as aluminum material. Europe '440 discloses depositing a silicon carbon barrier layer on a metal surface, between two metal layers to prevent interlayer diffusion, or between a metal and a subsequently deposited dielectric material to prevent diffusion of the metal into the dielectric material and insulate layers of wiring.

Wang et al. discloses a thermal CVD deposition of silicon oxide followed by a plasma enhanced CVD deposition of silicon oxide in the same processing chamber. Applicants disclose knowledge of the use of anti-reflective coatings (ARC) and photoresist materials in photolithographic processes for patterning a feature shape on a substrate surface and then etching the feature shape to form a feature definition. Applicants disclose knowledge that prior art anti-reflective coatings (ARC) have had high dielectric constants.

Somekh discloses depositing a carbon based etch stop, such as a diamond like amorphous carbon and fluorocarbon, or alternatively, silicon carbide, having a low dielectric constant in a method for forming a dual damascene structure. *Zhao* discloses depositing a etch stop over a low k dielectric layer, and the dielectric layer may comprise a variety of dielectric materials including silicon carbide.

Endo et al. provides no disclosure or suggestion of silicon carbide as a barrier layer, etch stop, or ARC, or depositing a silicon carbide layer with a low dielectric constant. *Endo et al.* further provides no disclosure or suggestion of depositing a first dielectric layer *in situ* on a silicon carbide layer or depositing a photoresist layer. Applicants also disclose that *Endo et al.* provides no disclosure of SiC as a barrier layer, etch stop, or ARC.

European Patent 0725440 does not disclose silicon carbide as an etch stop or anti-reflective coating as recited in one or more of the rejected claims. As disclosed in Applicants' specification, European Patent 0725440 (*Loboda* U.S. Pat. No. 5,818,071), is designed to accommodate a subtractive deposition in which the substrate deposition deposits the metal layer, then etches the metal and deposits the SiC into the etched

metal layer. Therefore, routine optimization of the silicon carbide barrier layer of European Patent 0725440 in view of the other references as asserted by the Examiner would not suggest or motivate depositing a silicon carbide etch stop or a silicon carbide anti-reflective coating as recited in one or more of the rejected claims. European Patent 0725440 further provides no disclosure or suggestion of depositing a first dielectric layer *in situ* on a silicon carbide layer or depositing a photoresist layer.

Further, *Wang et al.*, Applicants disclosure of knowledge, *Somekh* and *Zhao*, either alone or in combination with any other references, does not teach, show, or suggest depositing silicon carbide materials, either *in situ*, or with other dielectric materials. Additionally, *Wang et al.* and Applicants disclosure of knowledge, either alone or in combination with any other references, does not teach, show, or suggest depositing silicon carbide materials as barrier layers, etch stops, or as ARC films.

Endo et al., European Patent 0725440, *Wang et al.*, *Somekh* and *Zhao*, and Applicants disclosure of knowledge, either alone or in combination, do not teach, show or suggest depositing a silicon carbide layer, depositing a first dielectric layer *in situ* on the silicon carbide layer, and then depositing a photoresist layer, as recited in claim 14 and claims dependent thereon.

Endo et al., European Patent 0725440, *Wang et al.*, *Somekh* and *Zhao*, and Applicants disclosure of knowledge, either alone or in combination, do not teach, show or suggest depositing a silicon carbide barrier layer on the substrate, depositing a first dielectric layer *in situ* on the barrier layer, depositing an etch stop *in situ* on the first dielectric layer, depositing a second dielectric layer *in situ* on the etch stop, depositing a silicon carbide anti-reflective coating *in situ* on the second dielectric layer and depositing a photoresist layer on the silicon carbide anti-reflective coating, as recited in claim 26, and claims dependent thereon.

Therefore, *Endo et al.*, European Patent 0725440, *Wang et al.*, and Applicants disclosure of knowledge, either alone or in combination, do not teach, show or suggest claimed aspects of the invention. Withdrawal of the rejection is respectfully requested.

Claim 29 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of *Endo et al.* '150, Europe '440, *Wang et al. '947, Somekh* and *Zhao* as applied to claims 14-28, 30 and 31 above, and further in view of *Subrahmanyan et al.*

The Examiner asserts that it would have been within the scope of one of ordinary skill in the art to combine the teachings of *Endo et al.* '150, Europe '440, *Wang et al. '947, Somekh* and *Zhao* and *Subrahmanyan et al.* to achieve reduction of contact resistance by including a nitrogen/hydrogen plasma cleaning.

Endo et al. '150, Europe '440, *Wang et al. '947, Somekh* and *Zhao* are described above. *Subrahmanyan et al.* discloses a precleaning process for cleaning dielectric materials by a plasma of reactive gas such as oxygen, a mixture of CF_4/O_2, or a mixture of He/NF_3, with the plasma generated by a remote plasma source.

Subrahmanyan et al., either alone or in combination with *Endo et al.* '150, Europe '440, *Wang et al. '947, Somekh* and *Zhao*, does not teach, show or suggest depositing a silicon carbide barrier layer on the substrate, depositing a first dielectric layer *in situ* on the barrier layer, depositing an etch stop *in situ* on the first dielectric layer, depositing a second dielectric layer *in situ* on the etch stop, depositing a silicon carbide anti-reflective coating *in situ* on the second dielectric layer and depositing a photoresist layer on the silicon carbide anti-reflective coating, as recited in claim 26, and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the claimed aspects of the invention. Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

Keith M. Tackett
Registration No. 32,008
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd., Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)